

DM74LS132

Quad 2-Input NAND Gate with Schmitt Trigger Input

General Description

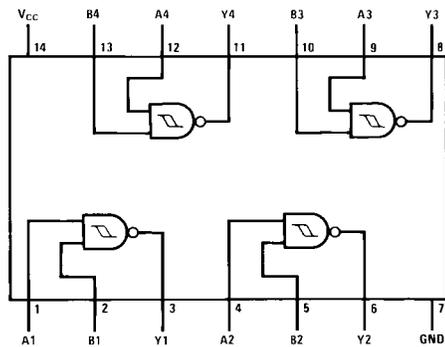
This device contains four independent gates each of which performs the logic NAND function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter free output.

Ordering Code:

Order Number	Package Number	Package Description
DM74LS132M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS132SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS132N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH Logic Level
L = LOW Logic Level

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{T+}	Positive-Going Input Threshold Voltage (Note 2)	1.4	1.6	1.9	V
V_{T-}	Negative-Going Input Threshold Voltage (Note 2)	0.5	0.8	1	V
HYS	Input Hysteresis (Note 2)	0.4	0.8		V
I_{OH}	HIGH Level Output Current			-0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = \text{Min}, I_I = -18 \text{ mA}$			-1.5	V
V_{OH}	HIGH Level Output Voltage	$V_{CC} = \text{Min}, I_{OH} = \text{Max}, V_I = V_{T-} \text{ Min}$	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	$V_{CC} = \text{Min}, I_{OL} = \text{Max}, V_I = V_{T+} \text{ Max}$		0.35	0.5	V
		$I_{OL} = 4 \text{ mA}, V_{CC} = \text{Min}$		0.25	0.4	
I_{T+}	Input Current at Positive-Going Threshold	$V_{CC} = 5V, V_I = V_{T+}$		-0.14		mA
I_{T-}	Input Current at Negative-Going Threshold	$V_{CC} = 5V, V_I = V_{T-}$		-0.18		mA
I_I	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}, V_I = 7V$			0.1	mA
I_{IH}	HIGH Level Input Current	$V_{CC} = \text{Max}, V_I = 2.7V$			20	μA
I_{IL}	LOW Level Input Current	$V_{CC} = \text{Max}, V_I = 0.4V$			-0.4	mA
I_{OS}	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 4)	-20		-100	mA
I_{CCH}	Supply Current with Outputs HIGH	$V_{CC} = \text{Max}$		5.9	11	mA
I_{CCL}	Supply Current with Outputs LOW	$V_{CC} = \text{Max}$		8.2	14	mA

Note 2: $V_{CC} = 5V$

Note 3: All typicals are at $V_{CC} = 5V, T_A = 25^\circ\text{C}$.

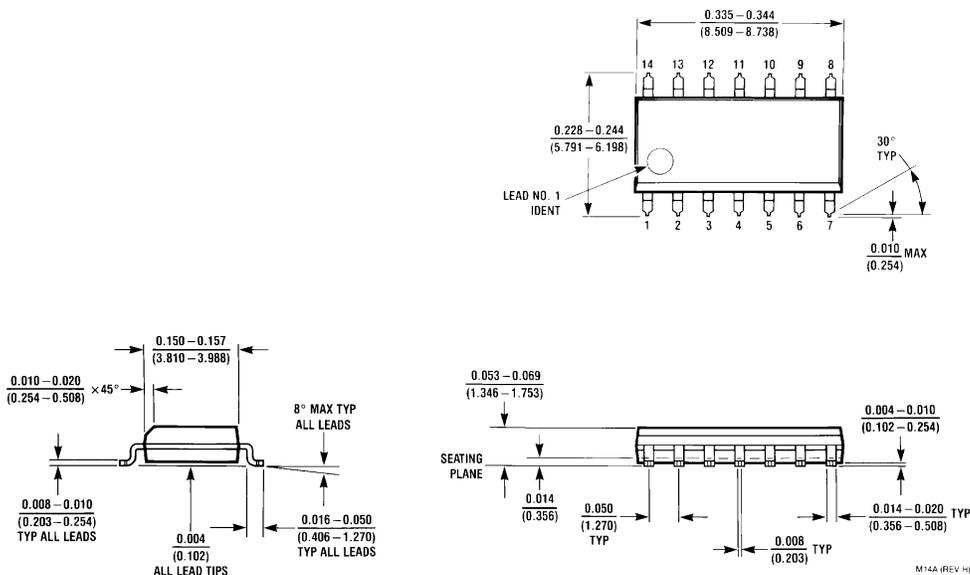
Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25^\circ\text{C}$

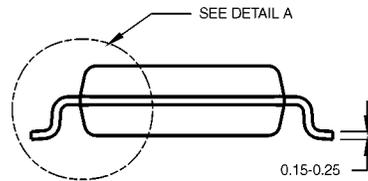
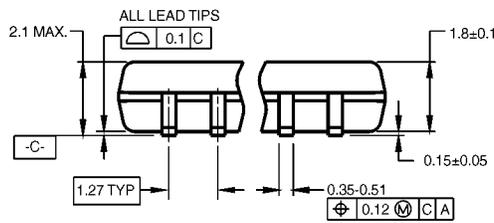
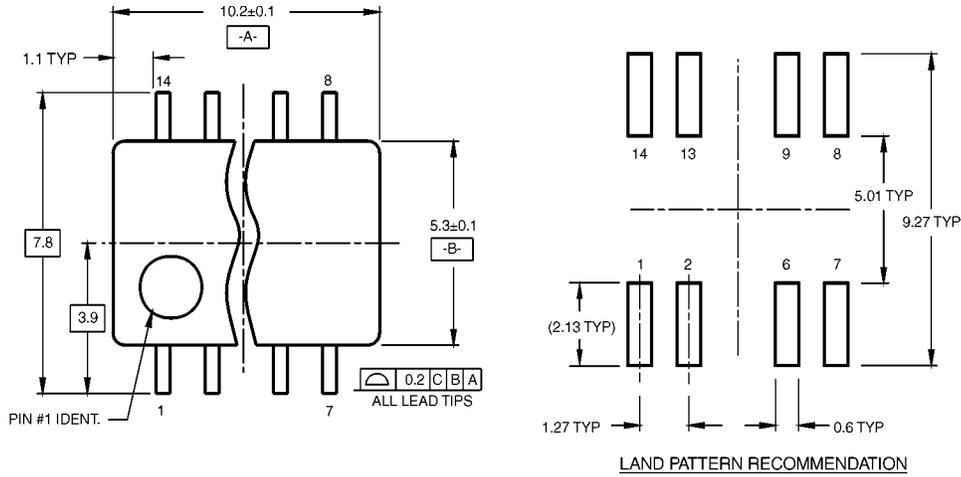
Symbol	Parameter	$R_L = 2 \text{ k}\Omega$				Units
		$C_L = 15 \text{ pF}$		$C_L = 50 \text{ pF}$		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	5	22	8	25	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	5	22	10	33	ns

Physical Dimensions inches (millimeters) unless otherwise noted



**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A**

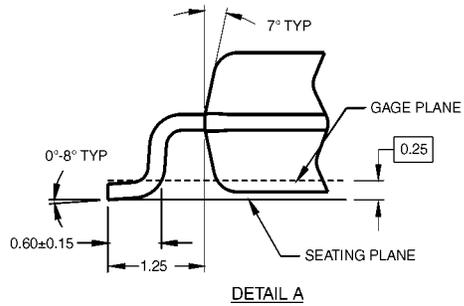
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

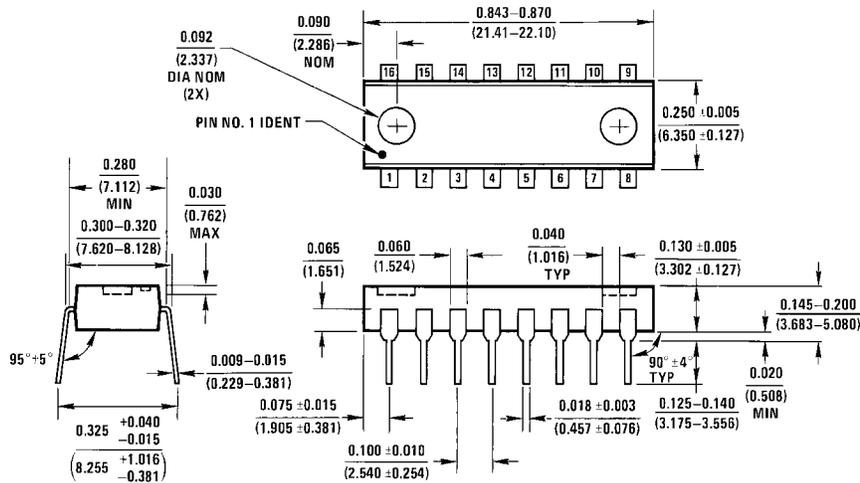
- NOTES:
 A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 B. DIMENSIONS ARE IN MILLIMETERS.
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1



**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
 Package Number M14D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



N16A (REV E)

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N14A

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