

# HCF4051

## Single 8-channel analog multiplexer/demultiplexer

#### Datasheet - production data



### Features

- Low "ON" resistance: 125 Ω (typ.)
- Over 15 V p.p signal-input range for V<sub>DD</sub> - V<sub>EE</sub> = 15 V
- High "OFF" resistance, channel leakage: ± 100 pA (typ.) at V<sub>DD</sub> - V<sub>EE</sub> = 18 V
- Binary address decoding on chip
- High degree of linearity: < 0.5 % distortion typ. at  $f_{IS}$  = 1 KHz,  $V_{IS}$  = 5  $V_{pp}$ ,  $V_{DD}$   $V_{SS} \ge$  10 V,  $R_L$  = 10 k $\Omega$
- Very low quiescent power dissipation under all digital control input and supply conditions:
  0.2 μW (typ.) V<sub>DD</sub> - V<sub>SS</sub> = V<sub>DD</sub> - V<sub>EE</sub> = 10 V
- Matched switch characteristics:  $R_{ON} = 5 \Omega (typ.)$  for V<sub>DD</sub> - V<sub>EE</sub> = 15 V
- Wide range of digital and analog signal levels: digital 3 to 20, analog to 20 V p.p.
- Quiescent current specified up to 20 V
- 5 V, 10 V and 15 V parametric ratings
- ESD performance
  - HBM: 2 kV
  - MM: 200 V
  - CDM: 750 V

- Input leakage current I<sub>I</sub> = 100 nA (max.) at V<sub>DD</sub> = 18 V, T<sub>A</sub> = 25 °C
- 100 % tested for quiescent current

### Applications

- Automotive
- Industrial
- Computer
- Consumer

### Description

The HCF4051 device is a monolithic integrated circuit fabricated in MOS (metal oxide semiconductor) technology available in SO-16 and PDIP-16 packages.

The HCF4051 analog multiplexer/demultiplexer is a digitally controlled analog switch having low ON impedance and very low OFF leakage current. This multiplexer circuit dissipates extremely low quiescent power over the full <sub>VDD</sub> - V<sub>SS</sub> and V<sub>DD</sub> - V<sub>EE</sub> supply voltage range, independent of the logic state of the control signals.

This device is a single 8-channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output. When a logic "1" is present at the inhibit input terminal all channels are off.

Table 1. Device summary										
Order code	Temperature range	Package	Packaging	Marking						
HCF4051M013TR	-55/+125 °C	SO-16	Tape and reel	HCF4051						
HCF4051YM013TR <sup>(1)</sup>	-40/+125 °C	SO16 (automotive version)	Tape and Teel	HCF4051Y						
HCF4051BEY	-55/+125 °C	PDIP-16	Tube	HCF4051BE						

1. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q002 or equivalent.

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This is information on a product in full production.

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## 1 Pin information





#### Table 2. Pin description

Pin no.	Symbol	Name and function
11, 10, 9	A, B, C	Binary control inputs
6	INH	Inhibit inputs
13, 14, 15, 12, 1, 5, 2, 4	0 to 7 channel IN/OUT	Independent inputs/outputs
3	COM OUT/IN	Common output/input
7	V <sub>EE</sub>	Supply voltage
8	V <sub>SS</sub>	Negative supply voltage
16	V <sub>DD</sub>	Positive supply voltage



## 2 Functional description

Input	"ON" channel (S)			
Inhibit	С	В	Α	"ON" channel (S)
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	Х	Х	Х	None

Table 3. Truth table













### 3 Electrical characteristics

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All voltage values are referred to  $V_{SS}$  pin voltage.

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	Supply voltage	-0.5 to +22	V
VI	DC input voltage	-0.5 to V <sub>DD</sub> + 0.5	V
I <sub>I</sub>	DC input current	±10	mA
Р	Power dissipation per package	500 <sup>(1)</sup>	mW
PD	Power dissipation per output transistor	100	mvv
T <sub>op</sub>	Operating temperature	-55 to +125	0°
T <sub>stg</sub>	Storage temperature	-65 to +150	

1. 500 mW at 65 °C; derate to 300 mW by 10 mW/°C from 65 °C to 85 °C.

Table 5. Recommended operating conditions
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Symbol	Parameter	Value	Unit
V <sub>DD</sub>	Supply voltage	3 to 20	V
VI	Input voltage	0 to V <sub>DD</sub>	v
T <sub>op</sub>	Operating temperature	-55 to 125	°C

		Test condition					Value				
Symbol Paran	Parameter	V <sub>IS</sub>	V <sub>EE</sub>	V <sub>EE</sub> V <sub>SS</sub>	V <sub>DD</sub>	T <sub>A</sub> = 25 °C			-55 to 125 °C		Unit
		(V)	(V)	(V)	(V)	Min.	Тур.	Max.	Min.	Max.	
	Quiescent device				5		0.04	5		150	
۱ <sub>L</sub>	current (all switches				10		0.04	10		300	μA
۰Ľ	ON or all switches OFF)	ON or all switches		15		0.04	20		600	μ	
	,				20		0.08	100		3000	
Switch											
					5		470	1050		1200	
R <sub>ON</sub>	Resistance	$0 \leq V_{I} \leq V_{DD}$	0	0	10		180	400		520	
					15		125	280		360	Ω
	Resistance $\Delta_{RON}$				5		10				32
D <sub>ON</sub>	(between any 2 of 4 switches)	$0 \leq V_{I} \leq V_{DD}$	V <sub>DD</sub> 0 0	0	10		10				
	switches)			15		5					
OFF <sup>(1)</sup>	Channel leakage current (all channels OFF) (COMMON O/I)		0	0	18		±0.1	100		1000	nA
OFF <sup>(1)</sup>	Channel leakage current (any channel OFF)		0	0	18		±0.1	100		1000	
CI	Input capacitance						5				
C <sub>O</sub>	Output capacitance		-5	-5	5		30				pF
CIO	Feedthrough						0.2				
Control (	address or inhibit)										
					5			1.5		1.5	
V <sub>IL</sub>	Input low voltage		V <sub>EE</sub> :	= V <sub>SS</sub>	10			3		3	
		= V <sub>DD</sub> through		÷1KΩ V <sub>SS</sub>	15			4		4	V
		<sup>1</sup> ΚΩ	I <sub>IS</sub> <	2μA II OFF	5	3.5			3.5		V
$V_{\text{IH}}$	Input high voltage	oltage		inels)	10	7			7		1
					15	11			11		
$I_{IH_{I}}I_{IL}$	Input leakage current	V <sub>1</sub> = 0/	'18 V		18		±10 <sup>-3</sup>	±0.1		±1	μA
CI	Input capacitance						5	7.5			pF

Table 6. DC specifications

1. Determined by minimum feasible leakage measurement for automating testing.



	Test condition							Value			Unit
Parameter	V <sub>EE</sub> (V)	<b>R</b> L (ΚΩ)	f <sub>l</sub> (KHz)	V <sub>I</sub> (V)	V <sub>SS</sub> (V)	V <sub>DD</sub> (V)		Min.	Тур.	Max.	
						5			30	60	
Propagation delay time (signal input to output)		200		V <sub>DD</sub>		10			15	30	ns
						15			11	20	
Frequency response channel "ON"	=V <sub>SS</sub>	1		5 <sup>(2)</sup>		10	V <sub>O</sub> at common OUT/IN		20		
(sine wave input) at 20 log V <sub>O</sub> /V <sub>I</sub> = -3 dB	- v <sub>SS</sub>			0.7		10	V <sub>O</sub> at any channel		60		
Feedthrough (all channels OFF)	=V <sub>SS</sub>	1		5 <sup>(2)</sup>		10	V <sub>O</sub> at common OUT/IN		12		MHz
at 20 log $V_0/V_1 = -40 \text{ dB}$	- v <sub>SS</sub>			5.7		10	V <sub>O</sub> at any channel		8		
Frequency signal crosstalk at 20 log $V_0/V_1 = -40 \text{ dB}$	= V <sub>SS</sub>	1		5 <sup>(2)</sup>		10	Between any 2 channels		3		
				2 <sup>(2)</sup>		5			0.3		
Sine wave distortion f <sub>IS</sub> = 1 KHz sine wave	$= V_{SS}$	10	1	3 <sup>(2)</sup>		10			0.2		%
2				5 <sup>(2)</sup>		15			0.12		
Control (address or inhib	it)										
	0				0	5			360	720	
Propagation delay:	0				0	10			160	320	
address to signal OUT (channels ON or OFF)	0				0	15	]		120	240	
	-5				0	5			225	450	
	0				0	5			360	720	
Propagation delay: inhibit	0	1			0	10	]		160	320	
to signal OUT (channel turning ON)	0	1			0	15			120	240	ns
	-10				0	5			200	400	
	0					5			200	450	
Propagation delay: inhibit to signal OUT (channel turning OFF)	0	10				10	]		90	210	1
	0	10				15	]		70	160	
-	-10					5	]		130	300	
Address or inhibit to signal crosstalk	0	10 <sup>(1)</sup>			0	10	V <sub>C</sub> = V <sub>DD</sub> - V <sub>SS</sub> (square wave)		65		mV peak

Table 7. Dynamic electrical characteristics  $(T_{amb} = 25 \text{ °C}, C_L = 50 \text{ pF}, \text{ all input square wave rise and fall time = 20 ns})^{(1)}$ 

1. Both ends of channel.

2. Peak-to-peak voltage symmetrical about (V\_{DD} - V\_{EE} ) /2.





#### Figure 4. Typical bias voltages

1. The ADDRESS (digital-control inputs) and INHIBIT logic levels are : "0" = V<sub>SS</sub> and "1" = V<sub>DD</sub>. The analog signal (through the TG) may swing from V<sub>EE</sub> to V<sub>DD</sub>.

#### Special considerations

Control of analog signals up to 20 V peak-to-peak can be achieved by digital signal amplitudes of 4.5 to 20 V (if  $V_{DD} - V_{SS} = 3 V$ , a  $V_{DD} - V_{EE}$  of up to 13 V can be controlled; for  $V_{DD} - V_{EE}$  level differences above 13 V, a  $V_{DD} - V_{SS}$  of at least 4.5 V is required).

For example, if  $V_{DD}$  = +5,  $V_{SS}$  = 0, and  $V_{EE}$  = -13.5, analog signals from -13.5 V to 4.5 V can be controlled by digital inputs of 0 to 4.5 V. In certain applications, the external load resistor current may include both  $V_{DD}$  and signal-line components. To avoid drawing  $V_{DD}$  current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 V (calculated from R<sub>ON</sub> values shown in *Table 6: DC specifications*). No  $V_{DD}$  current flows through R<sub>L</sub> if the switch current flows into lead 3.





1.  $C_L$  = 50 pF or equivalent (includes jig and probe capacitance)  $R_L$  = 200 K $\Omega$  $R_T$  = Z<sub>OUT</sub> of pulse generator (typically 50  $\Omega$ ).





Figure 6. Waveform 1: channel turned ON ( $R_L$  = 1 K $\Omega$ , f = 1 MHz; 50 % duty cycle)

#### Figure 7. Waveform 2: channel turned OFF (R<sub>L</sub> = 1 KW, f = 1 MHz; 50 % duty cycle)





### 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.



### 4.1 PDIP-16 (0.25) package information



#### Figure 8. PDIP-16 (0.25) package mechanical drawing

#### Table 8. PDIP-16 (0.25) package mechanical data

	Dimensions									
Symbol		mm		inch						
	Min.	Тур.	Max.	Min.	Тур.	Max.				
a1	0.51			0.020						
В	0.77		1.65	0.030		0.065				
b		0.5			0.020					
b1		0.25			0.010					
D			20			0.787				
E		8.5			0.335					
е		2.54			0.100					
e3		17.78			0.700					
F			7.1			0.280				
Ι			5.1			0.201				
L		3.3			0.130					
Z			1.27			0.050				



### 4.2 SO-16 package information



### Figure 9. SO-16 package mechanical drawing

#### Table 9. SO-16 package mechanical data

	Dimensions									
Symbol		mm		inch						
	Min.	Тур.	Max.	Min.	Тур.	Max.				
А			1.75			0.068				
a1	0.1		0.2	0.003		0.007				
a2			1.65			0.064				
b	0.35		0.46	0.013		0.018				
b1	0.19		0.25	0.007		0.010				
С		0.5			0.019					
c1			45°	(typ.)						
D	9.8		10	0.385		0.393				
E	5.8		6.2	0.228		0.244				
е		1.27			0.050					
e3		8.89			0.350					
F	3.8		4.0	0.149		0.157				
G	4.6		5.3	0.181		0.208				
L	0.5		1.27	0.019		0.050				
М			0.62			0.024				
S			8 ° (	max.)	•	•				



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## 5 Ordering information

Table	10.	Order	codes
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Order code	Temperature range	Package	Packaging	Marking
HCF4051M013TR	-55/+125 °C	SO-16		HCF4051
HCF4051YM013TR <sup>(1)</sup>	-40/+125 °C	SO16 (automotive version)	Tape and reel	HCF4051Y
HCF4051BEY	-55/+125 °C	PDIP-16	Tube	HCF4051BE

1. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q002 or equivalent.

### 6 Revision history

Date	Revision	Changes	
26-Oct-2012	2	Updated <i>Features</i> (added ESD values), added <i>Applications</i> . Updated <i>Table 1</i> (reformatted table, added order codes, temperature range, marking, updated package and packaging). Updated <i>Description</i> (unified part numbers, moved to page 2). Updated <i>Section 2</i> to <i>Section 4</i> (added titles and numbering). Updated <i>Table 6</i> (removed -40/+85° temperature range). Reformatted <i>Section 4</i> (added ECOPACK text, <i>Figure 8, Figure 9,</i> <i>Table 8</i> , and <i>Table 9</i> ). Minor corrections throughout document.	
30-Apr-2013	3	Updated <i>Features</i> (ESD values) Added <i>Section 5: Ordering information</i>	

Table 11. Document revision history	Table 11.	Document	revision	history
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